STACKED MICROELECTRONIC ASSEMBLIES AND METHODS OF MAKING SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims benefit of United States Provisional Patent Application No. 60/261,059 filed January 11, 2001, the disclosure of which is incorporated by reference herein.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to stacked microelectronic assemblies and methods of making such assemblies, to methods of forming such assemblies and to components useful in such assemblies.

[0003] Semiconductor chips are commonly provided as individual, prepackaged units. A standard chip has a flat, rectangular body with a large front face having contacts connected to the internal circuitry of the chip. Each individual chip typically is mounted in a package, which in turn is mounted on a circuit panel such as a printed circuit board and which connects the contacts of the chip to conductors of the circuit panel. In many conventional designs, the chip package occupies an area of the circuit panel considerably larger than the area of the chip itself. As used in this disclosure with reference to a flat chip having a front face, the "area of the chip" should be understood as referring to the area of the front face. In "flip chip" designs, the front face of the chip confronts the face of the circuit panel and the contacts on the chip are bonded directly to the circuit panel by solder balls or other connecting elements. The "flip chip" design provides a relatively compact planar arrangement; each chip occupies an area of the circuit panel equal to or slightly larger than the area of the chip front face. However, this approach suffers from cost and reliability problems. As disclosed, for example, in certain embodiments of commonly assigned U.S. Patents 5,148,265 5,148,266, and 5,679,977 the disclosures of which are

incorporated herein by reference certain innovative mounting techniques offer compactness approaching or equal to that of conventional flip chip bonding without the reliability and testing problems commonly encountered in that approach. A Package which can accommodate a single chip in an area of the circuit panel equal to or slightly larger than the area of the chip itself are commonly referred to as "chip size packages".

[0004] Besides minimizing the planar area of the circuit panel occupied by a microelectronic assembly, it is also desirable to produce a chip package that presents a low overall height or dimension perpendicular to the plane of the circuit panel. Such thin microelectronic packages allow for placement of a circuit panel having the packages mounted thereon in close proximity to neighboring structures, thus reducing the overall size of the product incorporating the circuit panel.

[0005] Various proposals have been advanced for providing plural chips in a single package or module. In a conventional "multi-chip module", the chips are mounted side-by-side on a single package substrate, which in turn can be mounted to the circuit panel. This approach offers only limited reduction in the aggregate area of the circuit panel occupied by the chips. The aggregate area is still greater than the total surface area of the individual chips in the module. It has also been proposed to package plural chips in a "stacked" arrangement, i.e., an arrangement where plural chips are placed one on top of another. In a stacked arrangement, several chips can be mounted in an area of the circuit panel that is less than the total area of the chips. Certain stacked chip arrangements are disclosed, for example, in certain embodiments of the aforementioned '977 and '265 patents and in U.S. Patent No. 5,347,159, the disclosure of which is incorporated herein by reference. U.S. Patent No. 4,941,033, also incorporated herein by reference, discloses an arrangement in which chips are stacked on top of

another and interconnected with one another by conductors on so-called "wiring films" associated with the chips.

[0006] Another approach is presented in commonly assigned U.S. Patents Nos. 6,121,676; 6,225,688; and U.S. Patent Application Serial No. 09/776,356 filed February 2, 2001, the disclosures of which are incorporated herein by reference. The stacked microelectronic assemblies disclosed certain preferred embodiments of these patents and application include a flexible substrate having a plurality of attachment sites and conductive elements and a plurality of chips connected thereto. The flexible substrate is folded so as to stack the chips in substantially vertical alignment with one another. The resulting stacked assemblies typically have at least one layer of flexible substrate for every one or two chips in the stack which adds to the overall thickness of the assembly.

[0007] Certain preferred embodiments of U.S. Patent No. 5,861,666, the disclosure of which is incorporated herein by reference, disclose an assembly of plural chip-bearing units vertically stacked one atop the other. Each unit includes a small panel or "interposer" and a semiconductor chip mounted thereto. The assembly also includes compliant layers disposed between the chips and the interposers so as to permit relative movement of the chips and interposers to compensate for thermal expansion and contraction of the components. The units are stacked so that the chips overlie one another, and are electrically interconnected with one another as, for example, by solder balls connecting conductive features of adjacent interposers to one another. The presence of an interposer in each unit contributes to the thickness of the stack.

[0008] Still further improvements in stacked chip assemblies would be desirable. Stacked chip assemblies should deal effectively with the problems associated with heat generation in stacked chips. Chips dissipate electrical power as heat during operation. Where chips are stacked one atop the other, it is

difficult to dissipate the heat generated by the chips in the middle of the stack. Also, chips and circuit panels undergo substantial thermal expansion and contraction during operation. Differences in thermal expansion and contraction can impose significant mechanical strain on elements of the assembly, including the electrical connections. Moreover, the assembly should be simple, reliable and easily fabricated in a cost-effective manner.

SUMMARY OF THE INVENTION

[0009] One aspect of the present invention provides stacked microelectronic assemblies having a low overall height. In preferred embodiments, according to this aspect of the invention, first and second microelectronic elements are provided, one stacked on top of the other, the first microelectronic element overlies a dielectric element. The microelectronic elements may be semiconductor chips or other elements. One or both of the microelectronic elements are electrically connected to terminals on the dielectric element. The preferred assemblies have an overall thickness above the terminals of less than 1.2mm. Preferably, joining units as, for example, solder balls, having a height of about 300 microns or less, more preferably 150 microns or less, are bonded to at least some of the terminals. The terminals on the dielectric element most preferably are movable relative to the first microelectronic element. In certain, more preferred embodiments, at least some of the terminals are disposed on a region of the dielectric element beneath the first microelectronic element. In the preferred assemblies according to this aspect of the invention, the various elements cooperate to provide an stacked chip assembly with both low height and high reliability. Because the terminals are movable relative to the bottom chip in the stack, the joining units will be subjected to relatively little deformation during manufacture and use. This facilitates the use of relatively

low-height joining units such as small solder balls while maintaining acceptable stresses in the joining units or solder balls and hence maintaining acceptable reliability in the finished product. The low height of the assembly above the terminals coacts with the low height of the joining unit to provide an assembly with low overall height.

[0010] A stacked assembly according to a further aspect of the invention provide includes a dielectric element having oppositely-facing first and second surfaces and a plurality of electrically conductive terminals exposed on the second surface. First and second microelectronic elements are provided, each with a respective face surface, back surface and plurality of contacts exposed on the face surface. The microelectronic elements are positioned in a back-to-back configuration, preferably with the first microelectronic element disposed between the second element and the first surface of the dielectric element. In this arrangement, the first microelectronic element is disposed in face-down orientation, with its face surface facing toward the dielectric element, whereas the second microelectronic element is disposed in face-up orientation, with its face surface facing upwardly, away from the dielectric element.

[0011] At least some of the contacts of the first and second microelectronic elements are electrically connected to the terminals of the dielectric element through first and second elongated leads, respectively. At least some of the terminals are movable with respect to the contacts of the first microelectronic element. Some preferred embodiments according to this aspect of the invention use employ wire bonds as first leads and as second leads. Particularly preferred structures according to this aspect of the invention can provide the required connections in a stacked structure using a dielectric element which incorporates all of the terminals and traces required to connect the terminals with

the leads in a single layer of metallic features. Thus, the dielectric element with traces and terminals thereon can be provided as a "single metal tape", using low-cost fabrication techniques. Still other preferred embodiments employ bond ribbons as the first leads and wire bonds as the second leads. The bond ribbons may be formed integrally with conductive traces on the dielectric element. Here again, the most preferred structures can be fabricated using a single layer of metallic features to form the traces, terminals and bond ribbons.

[0012] A stacked assembly according to a further aspect of the invention includes a dielectric element having conductive features thereon including elongated traces with terminals connected thereto, bond ribbons formed integrally with at least some of the traces, and bond pads formed integrally with others of the traces. First and second microelectronic elements such as semiconductor chips are provided, with the contact-bearing face surface of the first microelectronic element confronting the dielectric element and the second microelectronic element overlying the back surface of the first microelectronic element. Wire bonds connect the contacts of the second microelectronic element to the bond pads, and the bond ribbons extend to the contacts of the first microelectronic element. Preferably, the first and second microelectronic elements are substantially identical to one another and have each has its contacts disposed in a regions adjacent to an edge of the microelectronic element. More preferably, the contact-bearing edge regions of the first and second microelectronic elements are remote from one another.

[0013] A microelectronic assembly according to a further aspect of the invention also includes first and second microelectronic elements such as semiconductor chips. Each microelectronic element has a face surface, a back surface and first and second edges extending between the face and back

surfaces. The second microelectronic element overlies the first microelectronic element with the face surface of the second microelectronic element confronting a surface of the first microelectronic element. The microelectronic elements are staggered so that a first edge region of the second chip face surface adjacent the first edge of the second chip projects beyond first chip but the second edge of the second chip does not project beyond the first chip. For example, The two chips may be identical to one another, and the center of the second chip may be offset from the center of the first chip in a lateral direction, parallel to the plane of the face and back surfaces of the chips. The second chip has contacts within the projecting first edge region of its face surface. The first chip has contacts exposed on its face surface.

[0014] The assembly according to this aspect of the invention also includes a dielectric element having first and second surfaces, the first and second chips being disposed over said first surface of said dielectric element with the first chip between the dielectric element and the second chip. Electrically conductive features as, for example, traces and terminals, are provided on the dielectric element. Leads extend between at least some contacts of each chip and at least some of the conductive features on the dielectric element. The projecting edge region of the second chip face surface provides access to the second chip for connection of the leads.

[0015] In one preferred arrangement according to this aspect of the invention, the face surface of the second microelectronic element confronts the rear surface of the first chip, and both chips are disposed in face-down orientation. The contacts of the first chip may be disposed in a first edge region of the first chip front surface adjacent the first edge thereof, and the first edge of the first chip may be disposed adjacent the first edge of the second chip.

[0016] The edge regions of the first and second chips may project beyond a first edge of the dielectric element, and leads may extend around this edge of the dielectric element to conductive features of the dielectric element on the second surface. For example, where the conductive features on the dielectric element include bond pads exposed on the second surface of the dielectric element, wire bonds can extend around the first edge of the dielectric element.

[0017] Yet another aspect of the invention provides a stacked microelectronic assembly that includes a first subassembly, comprising a first microelectronic element and a first dielectric element, and a second subassembly, comprising a second microelectronic element and a second dielectric element. The first and second subassemblies are electrically interconnected with each other and arranged in a stacked arrangement relative to each other. The first dielectric element includes a plurality of terminals and first lands exposed on a surface that is opposite the surface that confronts the first microelectronic element. The second dielectric element has second lands exposed on a surface of the second dielectric element that is opposite the surface that confronts the second microelectronic element. The first and second subassemblies are arranged so that the respective land-bearing surfaces of the dielectric elements confront each other with the first lands overlying the second lands and being electrically connected thereto. Joining units connected to at least some of the terminals of the first subassembly project beyond the second subassembly. Preferably, the terminals of the first subassembly are disposed within a peripheral region of a dielectric element and the lands disposed within a central region, more preferably underlying the first microelectronic element. The lands of the first or second subassemblies are movable with respect to the respective microelectronic elements. As further explained

below, preferred assemblies according to this aspect of the invention provide a relatively compact structure and also facilitate testing of the individual subassemblies prior to joining of the subassemblies.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] FIG. 1A is a diagrammatic sectional elevational view of a stacked assembly according to one embodiment of the present invention.

[0019] FIG. 1B is a fragmentary, diagrammatic sectional view on an enlarged scale depicting the area indicated at 1B in FIG. 1A.

[0020] FIGS. 2A-2B are views similar to FIG. 1 but depicting other embodiments of the present invention.

[0021] FIG. 3 is a view similar to FIG. 2 but depicting yet another embodiment of the present invention.

[0022] FIG. 4 is side view similar to FIG. 1 but depicting another embodiment of the present invention.

[0023] FIGS. 5 is a fragmentary, diagrammatic view depicting steps of forming an electrical connection of a type illustrated in FIG. 4.

[0024] FIGS. 6, 7, and 8 are views similar to FIG. 1 but depicting further embodiments of the present invention.

[0025] FIGS. 9A and 9B are diagrammatic sectional elevational views of subassemblies used in an assembly according to another embodiment of the present invention.

[0026] FIG. 9C is a diagrammatic sectional elevational view of an assembly incorporating the subassemblies of FIGS. 9A and 9B.

[0027] FIG. 10 is a view similar to FIG. 10C but depicting another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0028] As shown in FIG. 1, a stacked microelectronic assembly 110 according to one embodiment of the present invention includes a first microelectronic element 10 and a

second microelectronic element 20. Microelectronic element 10 has a face surface 11 and a back surface 12 opposite the face surface. Electrical contacts 15 are exposed on face surface 11. Microelectronic element 20 is arranged similarly to microelectronic element 10, in that it has face surface 21, a back surface 22 opposite the face surface and electrical contacts 25 are exposed on face surface 21. In the embodiment of Fig. 1, each microelectronic element 10 and 20 is a conventional semiconductor chip. The contacts 15 on the first microelectronic element are disposed in a "area array" or array of contacts at substantially equal distances over the area of face surface 11, whereas the contacts 25 are disposed in two rows adjacent opposite edges of such surface.

[0029] The assembly also includes a dielectric element 50 has a first surface 51 and a second surface 52 with electrically conductive terminals 56 exposed on the second surface. As used in this disclosure, a statement that a conductive feature such as a terminal, contact, bonding pad or the like is "exposed on" a surface of a structure means that it is accessible to be electrically connected with another conductive element which approaches the surface. The conductive feature may be flush with the specified surface, may project outwardly from such surface, or may be recessed relative to such surface. For example, as best seen in Fig. 1B, terminals 56 are recessed from the second surface 52 of the dielectric element, but are exposed on the second surface 52 through holes 57 in the dielectric element. Preferably, dielectric element 50 comprises a layer of flexible material (Fig. 1A), such as a layer of polyimide, BT resin or other dielectric material of the type commonly utilized for making tape automated bonding ("TAB") tapes. Dielectric element 50 also includes additional conductive features including bond pads 55 exposed on first surface 51, conductive traces 53 as well as leads 70 in the form of bond ribbons formed integrally

with some of the traces. The dielectric element may further include a solder mask layer 58 (Fig. 1B) defining the first surface, with apertures or holes at bond pads 55. Traces connect the various conductive features to each other. Preferably, at least some of leads 70 are connected to at least some of the terminals 56, whereas at least some bond pads 55 are also connected to at least some of the terminals. Some or all of the bond pads may be connected with some or all of leads 70. Most preferably, all of the aforementioned conductive features on the dielectric element are formed from a single layer of metal. This avoids the need for precise registration between multiple layers of metallic features and formation of interconnections between such layers during manufacture of the dielectric element. Additional metallic features (not shown) such as conductive planes for use as ground planes or power distribution planes may be provide

[0030] Microelectronic element 10 is disposed over first surface 51 in a downwardly-facing orientation with face surface 11 confronting upwardly-facing first surface 51. Second microelectronic element 20 overlies first element 10 with face surface 21 in an upwardly-facing direction. One result of this arrangement is that back surfaces 12 and 22 confront each other in a "back-to-back" configuration. With regard to the present disclosure, terms such as "downwardly" or "upwardly" are used to describe directions that are opposed to each other without regard to any gravitational frame of reference. Similarly, terms such as "over" and "under", or "above" and "below" are used to describe the relative positions of elements of an assembly within the frame of reference of the assembly itself.

[0031] It is preferred, although not necessary to the invention, that microelectronic elements 10 and 20 are attached to each other by means such as adhesive layer 65. Adhesive 65 may be a die attach adhesive, and may comprised of

low elastic modulus material such as a silicone elastomer. However, where the two microelectronic elements are conventional semiconductor chips formed from the same material, they will tend to expand and contract in unison in response to temperature changes, and accordingly a relatively rigid attachment as, for example, a thin layer of a high-modulus adhesive or a solder can be employed.

[0032] Contacts 15 are electrically connected to the bond ribbon leads 70. The bond ribbons may be of the type described in United States Patent 5,518,964 , the disclosure of which is incorporated by reference herein. As disclosed in certain embodiments of the '964 patent, the bond ribbons may be initially formed in place on the first surface of the dielectric element, and may initially extend in the plane of such surface. The bond ribbons may be connected to the contacts 15 of the first microelectronic element, and may be deformed to the vertically-extensive disposition depicted in Figs. 1A and 1B by moving the first microelectronic element 10 and the dielectric element away from one another after bonding the ribbons to the contacts of the first microelectronic element. Related bond ribbon configurations and methods of forming bond ribbons are discussed in United States Patents 6,329,607; 6,228,686; 6,191,368; 5,976,913; and 5,859,472, the disclosures of which are also incorporated by reference herein.

[0033] Contacts 25 of the second microelectronic element 20 are electrically connected to bonding pads 55, and hence to terminals 56, by second leads 75 in the form of wire bonds. The wire bonds or second leads extend downwardly to the dielectric element and bonding pads past the edges of the first microelectronic element 10. The wire bonds may be formed by conventional wire bonding equipment and techniques. The wire bonding operation may be performed before the first microelectronic element 10 is moved away from the dielectric

element 50. For example, the first and second microelectronic elements may be attached to one another in back-to-back disposition by die attach material as discussed above; then the contacts 15 of the first microelectronic element 10 may be connected to the bond ribbons; then the wire bonding operation may be performed and finally the attached microelectronic elements may be moved away from the dielectric element 50. During the wire bonding operation, the face surface 11 of the element 10 abuts the dielectric element, which in turn may abut a support fixture (not shown) so as to provide a firm support during the wire bonding operation.

[0034] As illustrated in FIG. 1A, at least some of the terminals 56 are disposed beneath face surface 11 of microelectronic element 10. At least some of the terminals 56 are moveable with respect to the first microelectronic element 10 and hence with respect to at least some of contacts 15.

[0035] In preferred embodiments, stacked assembly 110 also includes a spacer layer 61 disposed between face surface 11 of microelectronic element 10 and first surface 51 of dielectric element 51. As disclosed in the '964 patent, the spacer layer may be formed by injecting a curable material around the leads during or after movement of the microelectronic element 10 away from the dielectric element. Desirably, spacer layer 61 is made of a compliant material that allows movement of dielectric element 50, and hence movement of terminals 56, relative to contacts 15. Preferred materials for such compliant layers include epoxies and silicones, with flexibilized epoxies and silicone elastomers being particularly preferred. The leads 70 and 75 are flexible to permit such movement. Assembly 110 may include an encapsulant 90 that covers elongated leads 75 and protects the microelectronic elements. In embodiments that do not include a separate spacer layer 61, the encapsulant may also be provided between the face surface 11 and first surface 51,

preferably surrounding leads 70, and may fill open spaces between microelectronic elements 10 and 20 Preferred encapsulants comprise flexibilized epoxies or silicone elastomers. Where the encapsulant is formed separately from the spacer layer, the encapsulant desirably has a modulus of elasticity that is greater than the modulus of elasticity of the spacer layer 61.

[0036] The stacked assembly may further include a plurality of joining units, such as eutectic solder balls 81. Solder balls 81 are attached to terminals 56, and hence are electrically interconnected to at least some of the bond pads 55, second leads 75 and second contacts 25, as well as to at least some of the first or ribbon leads 70 and first contacts 15. Other types of joining units such as solid-core solder balls, masses or balls of a diffusion-bonding or eutectic bonding alloy, masses of a conductive polymer composition, or the like may be employed.

[0037] In use, the assembly is mounted on a circuit panel such as a circuit board 91 having contact pads 93. The second surface 52 of the dielectric element faces downwardly toward the circuit board, and joining units 81 are bonded to the contact pads of the circuit board, thus connecting the contact pads to the microelectronic elements. The contact pads of the circuit board are connected by traces on or in the circuit board to the other elements of an electrical circuit which must coact with microelectronic elements 10 and 20. During the bonding operation, and during operation of the completed circuit board and circuit, differential thermal expansion and contraction of the circuit board and chips may occur. This may be caused by differences between the coefficients of expansion of the microelectronic elements and circuit board; by difference in temperature between the microelectronic elements and the circuit board; or by combinations of these factors. Such differential thermal expansion causes some or

all of the contact pads 93 to move relative to the microelectronic elements and contacts 15 and 25.

[0038] Movement of terminals 56 relative to the microelectronic elements, and particularly relative to first microelectronic element 10, relieves some or all of the stress which would otherwise be imposed on joining units 81 by relative movement of the terminals and contact pads.

[0039] Preferred combinations of the features described above allow the manufacture of a two-chip stacked assembly having thickness of less than 1.2 mm above the terminals 56. More preferably, such a thickness will be 0.7 mm (700 microns) or less.

[0040] In preferred embodiments of the present invention, joining units or solder balls 81 have a height of about 300 microns or less; more preferably, about 200 microns or less, and most preferably about 150 microns or less. Thus, the overall height of the assembly above the circuit panel after assembly, including the height of the joining units, most preferably is about 1.5 mm or less, and most preferably about 1.3 mm or less. Joining units having such low heights, also known as "fine pitch" joining units, may be used to beneficial effect with assemblies wherein the terminals are moveable with respect to the microelectronic elements and relative to the contacts on the microelectronic elements. As discussed above, this movability, relieves the mechanical strain or deformation generated by differential thermal expansion of the microelectronic elements. Some of the deformation may also be relieved by flexure of the joining units connecting the assembly to a circuit panel, such as a printed circuit board. Larger joining units can flex to a greater extent than smaller ones and, therefore, relieve a greater amount of deformation without failure due to fatigue of the joining units. In preferred embodiments of the present invention, the movement the terminals relative to microelectronic elements relieves a

significant portion of such deformation, allowing the use of relatively small joining units while still maintaining acceptable levels of reliability.

[0041] An assembly 120 according to a further embodiment of the invention, depicted in FIG. 2A, is generally similar to the assembly of FIGS. 1A-1B, but includes a a third microelectronic element 30. Element 30 is disposed over microelectronic element 20 with its contact-bearing face surface 31 facing in an upward direction, away from microelectronic element 20 and away from dielectric element 50. Third element 30 has at least one horizontal dimension smaller than the corresponding dimension of second element 20, so that contacts 25 of element 20 are exposed. Back surface 32 of third element 30 confronts face surface 21 of second element 20. Preferably, back surface 32 is attached to face surface 21 by an adhesive layer or other attachment as discussed above with reference to die attach layer 65. Contacts 35 are electrically connected to additional bond pads 55 by wire bonds 76.

[0042] The assembly 121 of FIG 2B is also generally similar to the assembly of FIGS. 1A-1B, but has a third microelectronic element 30 mounted below the dielectric element 50. The contact-bearing or face surface 31 of third microelectronic element 30 confronts second surface 52 of dielectric element 50. Ribbon leads 70′ connect contacts 35 to conductive features 59 exposed on second surface 52. These conductive features 59 may be traces formed integrally with ribbon leads 70, and may be connected with the other traces and conductive elements of the assembly, including terminals 56. Preferably, terminals 56′ and joining units 82′ mounted to such terminals are located in a peripheral region of second surface 52, whereas the third microelectronic element 30 and conductive features 59 are located in a central region thereof. Because element 30 is disposed on the same side of

dielectric element 50 as the joining units, joining units 82 must be large enough to project beyond the third element to contact the contact pads 93' of the circuit board or other circuit panel. However, because the third microelectronic element is accommodated within the height occupied by the joining units, the overall height of the assembly still can be the same as or less than the height of an assembly having the third microelectronic element mounted atop the second microelectronic element.

[0043] FIG. 3 illustrates another preferred embodiment 130 wherein the first microelectronic element includes two individual semiconductor chips or other individual components 40a,40b in place of the unitary chip 10 used in FIG. 1. Components 40a,40b are disposed adjacent to each other in a face-down configuration over dielectric element 50. Second microelectronic element 20 desirably is disposed over at least a portion of each component 40a,40b. In further variants, the first microelectronic element may include more than two components. Alternatively or additionally, the unitary second microelectronic element 20 can be replaced by an assemblage of two or more components disposed side-by-side.

[0044] FIG. 4 illustrates a preferred stacked assembly 140, similar to the assemblies of FIGS. 1A and 1B, but having the contacts 15 of microelectronic element 10 disposed within a central region of face surface 11. For example, contacts 15 may be formed as one or two parallel rows adjacent the center of face surface 11. These contacts electrically connected to dielectric element 150 by elongated ribbon leads 154 which are formed from metallized layer 157 of dielectric element 150. Here again, the ribbon leads desirably are formed integrally with traces or other conductive features on the dielectric element. Preferably, bond pads 155, and terminals terminals 156, as well as conductive traces used to provide

interconnections between conductive features, are formed as parts of a single metallic layer 157.

[0045] The dielectric element 150 includes an aperture or slot 185 which is aligned with the contacts 15. Ribbon leads 154 may be conventional leads of the type commonly used in tape automated bonding or "TAB" assemblies. As manufactured, the ribbon leads 154 project over the aperture or slot 185. During manufacture, the ribbon leads are engaged by a bonding tool such as a thermosonic or ultrasonic bonding tool, and forced into engagement with contacts 15. More preferably, ribbon leads 154 are formed in accordance with United States Patents 5,787,581; 5,915,752 and 5,977,618, the disclosures of which are also incorporated by reference herein. As described in greater detail in certain embodiments of those patents, and as schematically shown in FIG 5, the ribbon leads 154 as initially fabricated may include a bond section 154a that extends over slot or aperture 185. In a preferred method, bond section 154a may have a notch or other weakened portion therein to provide a fracture point 154b. A bonding tool is then inserted to break bond ribbon 154a and push the broken end to the position shown in broken lines at 154' making an electrical connection with contact 15 on face surface 11.

[0046] In the diagram of Fig. 4, the metallization layer 157 is depicted as lying on the second surface of dielectric element 150, i.e., the surface facing away from the microelectronic elements. In such a configuration, the dielectric element can incorporate apertures (not shown) at the bond pads 155 to expose the bond pads on the first surface of the dielectric element and facilitate connection of wire bonds 75. Alternatively or additionally, the metallization layer may be formed on the first surface of the dielectric element. Less preferably, conductive vias may extend through the dielectric element from traces on the second surface to bond pads on the first surface.

[0047] In an assembly according to a further embodiment 160, illustrated in FIG. 6, contacts 15 are electrically connected to bond pads 259 exposed on the second surface 251 of dielectric element 250 by elongated first leads 78 in the form of wire bonds. Leads 78 extend through aperture 285 which penetrates the dielectric element 250 to expose contacts 15. As depicted, spacer layer 61 is single pad that is also penetrated by aperture 285, but two of separate pads disposed on opposite sides of aperture 285 may be used to provide open space in alignment with the aperture. Preferably, leads 78 are covered by encapsulant 95. More preferably, encapsulant 95 fills aperture 285. The material used for encapsulant 95 may be the same as that used for encapsulant 90 or else different materials may be used.

[0048] Because bond pads 259 are exposed at the second surface 252, on the opposite side of dielectric element 250 from microelectronic element 10, leads 78 also extend beyond second surface 252. Joining units 282 must extend beyond the leads and any additional thickness provided by encapsulant 95 to be effective in connecting assembly 160 to a printed circuit board or other substrate. That is, the height A of the joining units 282 is equal to or, preferably, greater than, the height B of the encapsulant, both as measured from second surface 252 of the dielectric layer.

[0049] Dielectric element 250 is illustrated as having two layers of metallization, also known as a two metal tape, with conductive features on first surface 251, such as bond pads 255, being formed separately from conductive features on second surface 252, such as terminals 256 and bond pads 259. The metallic layers are connected to each other by vias 253 or other electrically conductive structures.

[0050] A stacked structure 300 depicted in FIG. 7 comprises a first microelectronic element in the form of a semiconductor chip 310 having contacts 315 and a second microelectronic

element in the form of a semiconductor chip 320 having contacts 325. Preferably, microelectronic elements 310 and 320 are substantially identical to one another. Microelectronic element 310 has a face surface 311; a back surface 312 opposite the face surface; a first edge 313 extending between the face and back surfaces and a second edge 314, on the side of the element opposite from edge 313, the second edge also extending between the face and back surfaces. Electrical contacts 315 are exposed on face surface 311, within a first edge region of the face surface adjacent first edge 313. The second microelectronic element has a similar face surface 321; a back surface 322 opposite the face surface; first edge 313 extending between the face and back surfaces; and second edge 314. Here again, the electrical contacts 325 are exposed on an edge region of face surface 321 adjacent the first edge 323 of the second element.

[0051] Chip 320 overlies chip 310, which is disposed between chip 320 and dielectric element 350. Face surface 321 of chip 320 faces downward toward dielectric element 350. Face surface 311 of the first chip 310 faces downward toward the dielectric element, so that face surface 321 confronts back surface 312 in a "front-to-back" configuration. The contact-bearing edge region of chip 320 projects beyond the first edge 313 of first chip 310. It is preferred, although not necessary to the invention, that chips 310 and 320 are attached to each other by means such as adhesive layer 365, similar to the adhesive layer 65 of FIG. 1.

[0052] Dielectric element 350 is, preferably, of the same single-metal type as has been described for the embodiments of FIG. 1. Element 350 has a first surface 351 and a second surface 352 with electrically conductive terminals 356 exposed on the second surface through a solder mask 358. Bond pads 359 are also exposed on second surface 352 in an edge region adjacent a first edge 353 of dielectric element 350.

[0053] The contact-bearing edge regions of chips 310,320 are oriented in a staggered formation, and both of these edge regions extend beyond the first edge 353 of the dielectric element nearest the bond pads. Such arrangements create relatively short distances between the contacts and the nearest bond pads. That is, chips 320 and 310 are oriented so that contacts 315,325 and bond pads 359 are present at the same end of assembly 300. The chips are staggered so that the edge region containing contacts 315 extends beyond edge 353 of dielectric element 350 and the edge region containing contacts 325 extend beyond both the region of contacts 315 and the region of bond pads 359. This results in the second edge 314 of chip 310, which is opposite edge 313, projecting beyond edge 324 of chip 320. Stated another way, the second edge 324 of the second chip 320 does not project beyond chip 310. Contacts 315 and 325 are electrically connected to bond pads 359 by elongated leads 370 and 375, respectively. Preferably, leads 370,375 are wire bonds. This particularly preferred embodiment provides economical bond formation. All of the bonds can be formed in a single wire-bonding setup, without reorienting the assembly. Moreover, the wire bonds do not extend upwardly beyond the second chip 320. Although the wire bonds and the encapsulant covering the wire bonds project downwardly beyond the dielectric layer 350, this does not add to the height of the assembly provided that the height B of the encapsulant is less than or equal to the height A of the joining units 381. In further variants, the same staggered arrangement of chips can be used with other types of bonding as, for example, with ribbon leads projecting from the dielectric layer.

[0054] In preferred embodiments, stacked assembly 310 also includes a spacer layer 361 disposed between chip 310 and first surface 351 of dielectric element 350. More preferably,

spacer layer 361 is a compliant layer. Such spacer layers have been discussed with respect to the embodiment of FIG. 1.

[0055] Assembly 310 may also include an encapsulant 390 that covers elongated leads 370,375. In embodiments that do not include a separate spacer layer 361, the encapsulant may also be provided between chip 310 and first surface 351, and may fill open spaces adjacent chips 310 and 320 and dielectric element 350. Preferred encapsulants are similar to those discussed with respect to the embodiment of FIG. 1.

[0056] Preferred combinations of the features described above allow the manufacture of a two-chip stacked assembly such as assembly 300 having a thickness of less than 700 microns above terminals 356.

[0057] Another preferred embodiment of a stacked assembly having a particularly low height is illustrated in FIG. 9. Preferably, microelectronic elements 410 and 420 are semiconductor chips that are substantially identical to one another. Chip 410 has contacts 415 exposed on a face surface 411, preferably disposed within a region adjacent three, more preferably two, and most preferably one, edges. In the preferred embodiment of FIG. 9, contacts 415 are disposed within a region adjacent first edge 413. Chip 410 also is provided with a second edge 414 opposite edge 413. Chip 420 preferably is substantially similar to chip 410, having contacts 425 exposed on a face surface 411 within a region adjacent a first edge 413, which is opposite a second edge 414. Chip 420 overlies chip 410, which is disposed between chip 420 and dielectric element 450 with face surface 411 confronting dielectric element 450. Chips 410 and 420 preferably are arranged in a "back-to-back" configuration, similar to that discussed for microelectronic elements 10 and 20 of FIG. 1, with face surface 411 confronting dielectric element 450 and face surface 421 facing away from the dielectric element. Preferably, chips 410

and 420 are attached to each other by means such as adhesive layer 465.

[0058] Dielectric element 450 is, preferably, of the same single-metal type as has been described for the embodiments of FIG. 1. The dielectric element is provided with conductive features, preferably including bond pads such as bond pads 455 exposed on first surface 451 and terminals 456 exposed on second surface 452 through openings in solder mask 458, the various conductive features being interconnected by traces and bond ribbons formed from the metallic layer.

[0059] Contacts 415 preferably are connected to bond ribbons leads 454, which, more preferably, are integral with the traces. Leads 454 may be made by the methods discussed above with regard to leads 154. Contacts 425 preferably are electrically connected to bond pads 455 by wire bonds 475. In preferred embodiments, at least some of the bond pads 455 are movable with respect to contacts 425. Wire bonds may be formed as discussed above.

[0060] In the preferred embodiment of FIG. 9, first edge 413 of chip 410 is disposed adjacent to second edge 424 of chip 420 so that contacts 415 and 425, respectively are near opposite ends of assembly 400. Other orientations of edges 413,414 relative to edges 423,424 are also within the scope of the preferred embodiments.

[0061] Assembly 400 preferably is provided with a spacer layer disposed between chip 410 and first surface 451 of dielectric element 450, illustrated as a multiplicity of compliant pads or nubbins 481. The assembly is provided, preferably, with encapsulant 490 surrounding the chips and bond wires, as also has been discussed herein. The encapsulant may penetrate between the nubbins to form a compliant spacer layer including both the nubbins and the encapsulant.

[0062] As depicted in FIG. 9, the stacked assembly may further include a plurality of joining units connected to

terminals 456. Low-height solder balls may be used, as has been discussed with respect to FIG. 1. Solder bumps 481, which are not full spherical balls, also may be used as joining units, typically being from about 110-150 microns in height.

[0063] In a further embodiment (FIGS. 10A-10C), the present invention provides stacked microelectronic assemblies comprising a first microelectronic subassembly 500 and a second microelectronic subassembly 600 that are electrically interconnected.

[0064] As depicted in Figure 10A, first microelectronic subassembly 500 comprises a first microelectronic element, such as a semiconductor chip, a plurality of semiconductor chips or a semiconductor wafer. Preferably, microelectronic assembly 510 has a face surface 511 with a plurality of first contacts (not shown) exposed thereon. First subassembly 500 also includes a first dielectric element 550 having a first surface 551 and a second surface 552. Dielectric element 550 may comprise a single-metal or bimetal tape; preferably, a single metal tape as discussed herein. Dielectric element 550 further comprises a plurality of first terminals 556 and first lands 555 exposed on second surface 552. In more preferred embodiments, terminals 556 are disposed in a peripheral region of dielectric element 550 and first lands 555 are disposed in a central region of the dielectric element.

[0065] Microelectronic element 510 overlies first surface 551, preferably in a face-down orientation with face surface 511 confronting first surface 551. At least some of the first contacts are electrically connected to at least some of the conductive features on first surface 551. In assembly 500, the connections are made through leads 554, the formation of which is discussed with respect to the embodiment of FIG. 5. The use of other types of leads, such as wire bonds discussed above, are also within the scope of the

preferred embodiments related to FIGS. 10-11. Use of ribbon leads such as leads 554 are preferred to minimize the overall thickness of the subassembly.

[0066] Preferably, first lands 555 are disposed so as to underlie microelectronic element 510. It is particularly preferred that at least some of terminals 556 are movable with respect to microelectronic element 510, for reasons discussed with respect to the stacked assembly of FIG. 1 and other embodiments of stacked assemblies disclosed herein.

[0067] Second microelectronic subassembly 600, depicted in FIG. 10B, comprises a second microelectronic element 620 and a dielectric element 650. Although second subassembly 600, as depicted, may be of similar construction to first subassembly 500, its preferred embodiments will be restricted to those having a particularly small thickness and areal extent substantially less than that of first subassembly 500. These restrictions are preferred so that subassembly 600 may fit within the terminal array of first subassembly 500 while minimizing the size of the joining units required to make an effective stacked assembly as illustrated in 10C.

[0068] Microelectronic element 620 preferably is a semiconductor chip having a face surface 611 with a plurality of second contacts (not shown) exposed thereon. Second subassembly 600 also includes a second dielectric element 650 having a first surface 651 and a second surface 652. Dielectric element 650 may comprise a single-metal or bimetal tape; preferably, a single metal tape as discussed herein. Dielectric element 650 further comprises a plurality of second lands 655 exposed on second surface 652. As will be obvious to those skilled in the art, the presence of terminals on the second subassembly is not necessary to the invention. The lands 655 desirably are movable with respect to element 620.

[0069] Microelectronic element 620 overlies first surface 651, preferably in a face-down orientation with face

surface 611 confronting first surface 651. At least some of the second contacts are electrically connected to at least some of the conductive features on first surface 651. Electrical connections between the second contacts and the dielectric element may be made by any suitable means disclosed herein.

[0070] Preferably, second lands 655 are disposed so as to underlie microelectronic element 620. It is particularly preferred that at least some of lands 655 are movable with respect to microelectronic element 620

[0071] As with other stacked assemblies disclosed herein, microelectronic subassemblies 500 and 600 preferably are provided with spacer layers 561,661 between microelectronic elements 510,610 and the respective first surfaces 551,651. The spacer layers may be compliant layers, in the form of a single pad or a plurality of pads or nubbins 561,661. Subassemblies 500 and 600 may also be provided with an encapsulant 590,690 surrounding the element and leads. Preferred materials and implementation of spacer layers and encapsulants have been discussed with respect to the embodiments of other stacked assemblies disclosed herein. The encapsulants 590,690 may be of the same materials as each other, or different materials may be used. Similarly, the spacer layers 561,661 may be of the same or different materials or construction, depending on the specific requirements of a selected embodiment.

[0072] First assembly 500 and second assembly 600 are electrically interconnected to form a stacked microelectronic assembly, such as that depicted in FIG. 10C, with second surface 552 and second surface 652 confronting each other. At least some of first lands 555 are electrically connected to at least some of and second lands 655, thereby providing electrical interconnections between the subassemblies. Preferably, the first lands overlie the second lands and are

joined thereto. Any suitable method may be used to join the respective lands one to another or to provide the electrical connections. The preferred method of doing so is to solder-bond the first lands to their respective second lands. The individual subassemblies may be tested prior to joining the subassemblies, as by engaging the terminals and/or lands with a test fixture prior to joining the assemblies with one another.

[0073] The stacked assembly of subassemblies 500,600 may further include a plurality of joining units, such as solder balls 581, which are connected to terminals 556 of first subassembly 500 and electrically interconnected, directly or indirectly, to first lands 555. The joining units must be sufficiently large so that they project from terminals 556 on second surface 552 beyond second assembly 600. That is to say, the height A of the joining units must be greater than the distance B from second surface 552 to the surface of second subassembly 600 that is furthest from surface 552. It is therefore beneficial to provide a second subassembly having the smallest thickness compatible with the intended purpose of the stacked assembly to minimize the necessary height of the joining units and, thus, the overall height of the assembly. Preferably, the elements of subassemblies 500 and 600 are selected to produce a stacked assembly having an overall thickness of about 1 mm or less, more preferably, about 700 microns or less, excluding the height of any joining units.

[0074] Although FIG. 9C depicts a particularly preferred embodiment wherein the centers of the first and second assemblies are aligned, the present invention also includes embodiments where the first assembly overlies some or all of the second assembly but the centers of such assemblies are not aligned. It is preferred that the second subassembly fit within the planar area of the first assembly. More

particularly, it is preferred that the second subassembly fit within the array of terminals on first surface 552.

[0075] As depicted in FIG. 10, the first subassembly may comprise microelectronic elements of other types than that depicted as subassembly 500. As an example, FIG. 10 illustrates a stacked package wherein the first subassembly 701 is of the same general type as the stacked assembly 300 discussed above with reference to FIG. 7. Also, any suitable microelectronic element may be substituted for first element 510 as long as first lands 555 and other suitable conductive features and connections are provided with dielectric element 550. Other microelectronic elements may be used in place of second element 620 consistent with the limitations of thickness and planar area discussed herein.

[0076] As these and other variations and combinations of the features discussed above can be utilized without departing from the present invention as defined by the claims, the foregoing description of the preferred embodiments should be taken by way of illustration rather than by way of limitation of the claimed invention.